Claims

We claim:

1. A ferroelectric memory array comprising:

a plurality of memory pages each formed of a plurality of ferroelectric memory cells supplied by common word lines;

status memory cells connected to each of the plurality of memory pages, each status memory cell storing the status of the memory page to which it is connected; and

a plurality of sense amplifiers each receiving inputs from a pair of bit lines, each bit line of the pair receiving inputs from ferroelectric memory cells from a plurality of the memory pages, the sense amplifiers writing back data into the memory cells and status cells in reversed states following read operations.

2. The ferroelectric memory array of Claim 1, wherein during read operations pairs of bit lines are directly connected to the sense amplifier and during write back pairs of bit lines are intersected.

3. The ferroelectric memory of Claim 1, further comprising a pair of imprint status bit lines connecting status memory cells together to provide input to an imprint status amplifier, the imprint status amplifier providing outputs to XOR gates of the sense amplifiers to provide logical data from the memory array which does not change when the physical data is reversed.

4. The ferroelectric memory of Claim 1, wherein the sense amplifier is comprised of a pair of inverters.